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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,110	09/09/2003	Anthony I-Chih Chou	FIS920030228US1	2109

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INTERNATIONAL BUSINESS MACHINES CORPORATION
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EXAMINER

KESHAVAN, BELUR V

ART UNIT	PAPER NUMBER
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2825

DATE MAILED: 04/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/605,110

Applicant(s)

CHOU ET AL.

Examiner

Belur V Keshavan

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 09 September 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3,5,7,9,10,12,15 and 20 is/are rejected.
- 7) ☒ Claim(s) 2,4, 6,8, 11, 13, 14, 16, 17, 18 and 19 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Drawings

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the following features must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

In claim 4, the feature “ forming a capacitor dielectric mask over said NFET area and said PFET area prior to beginning nitridation of a capacitor dielectric layer in a capacitor region, then performing capacitor dielectric nitridation thereof, and immediately thereafter removing said capacitor dielectric mask, and forming an FET mask over a previously formed capacitor region prior to beginning nitridation of said gate oxide layer in said NFET area and said PFET area, then performing FET gate dielectric nitridation thereof, and immediately thereafter removing said FET mask” is not shown in the drawings.

In claim 11, the feature “ forming a capacitor dielectric mask over said NFET area and said PFET area prior to beginning nitridation of a capacitor dielectric layer in a capacitor region, then performing capacitor dielectric nitridation thereof, and immediately thereafter removing said capacitor dielectric mask, and forming an FET mask over a previously formed capacitor region prior to beginning nitridation of said gate oxide layer in said NFET area and said PFET area, then performing FET gate dielectric nitridation thereof, and immediately thereafter removing said FET mask” is not shown in the drawings.

Therefore, the above features must be shown or the features canceled from the claims 4 and 11. No new matter should be entered.

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A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Objection To Specification

The specification is objected under 37 CFR 1.75(d) as failing to disclose an equal concentration of nitrogen in NFET and PFET areas. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 3, 7, 10 and 15 are rejected under 35 U.S.C. 112 second paragraph.

In claim 1, the nitrogen concentration in PFET and NFET gate oxide areas are different and in claims 3 and 10 the nitrogen concentration in PFET and NFET gate oxide areas are the same. Therefore a non-sequitor exists.

Claims 7 and 15 are rejected as being dependent upon indefinite claim.

Claims 3 and 10 recites the limitation "the other of said regions" in lines 4 and 12. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

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This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 5, 9, 12 and 20 are rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Trivedi et al. (U. S. Patent 6,541,395).

Regarding claims 1, 5, 9, 12 and 20 Trivedi et al. disclose the following:

In column 3 lines 24-63, and figure 1-7 a method of forming CMOS semiconductor materials with a PFET area (12) and a NFET area (14) formed on a semiconductor substrate (10).

In column 2 and lines 20-21, 29-30 and lines 45-52, a PFET gate dielectric (28) and a NFET gate dielectric (32) composed of silicon oxide with different degrees of nitridation.

In column 5 lines 41-44, Trivedi et al. also disclose that NFET gate dielectric layer and PFET gate dielectric layer can have same thickness.

Trivedi et al. do not disclose specifically nitridation of NFET gate dielectric. However in column 5 and lines 36-37, Trivedi et al. disclose that NFET gate dielectric with nitrogen concentration less than or equal to 0.1% molar and in column 2 and lines 48-50, PFET gate dielectric with nitrogen concentration of 0.1% molar to 10% molar. Therefore nitridation occurring in some form on NFET gate dielectric is at least suggested in Trivedi et al. Trivedi et al. also disclose that nitrogen concentration in PFET gate dielectric and in NFET gate dielectric

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are different and nitrogen concentration in PFET gate oxide layer is higher than that of NFET gate oxide layer.

It would have been obvious to one having an ordinary skill in the art at the time the invention was made to incorporate teachings of Trivedi et al. in forming a semiconductor device with NFET and PFET devices with the object of optimizing the electrical properties of thin gate dielectrics of PFET and NFET devices.

Claims 2, 4, 6, 8, 11, 13, 14, 16, 17, 18 and 19 are objected to as being dependent upon a base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The primary reason for the indication of allowability of Claims 2, 4, 6, 8, 11, 13, 14, 16, 17, 18 and 19 is the inclusion therein, in combination as currently claimed, of the limitation of a method of forming CMOS semiconductor materials with PFET area and NFET area comprising capacitor wherein the properties of the gate dielectric are tuned with different levels of nitridation of the gate dielectric.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Belur V Keshavan whose telephone number is 571-272-1894. The examiner can normally be reached on 8-4:30 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Bvk. *Bvk*
March 25, 2004.

Belur V. Keshavan.
Examiner, Art Unit 2825.

Matthew Smith
MATTHEW SMITH
FEDERAL BUREAU OF PATENT EXAMINATION
TECHNOLOGY CENTER, 2000